Application

for

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Title:

Active DC Output Control for Active Control of Leakage in Small Geometry Integrated Circuits

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to a co-pending U.S. patent application Ser. No. 10/294,842, filed on 11/13/2002; entitled "Active DC Output Control and Method for DC/DC Converter" by Myers et al., owned by the assignee of this application and incorporated herein by reference.

Field of Invention

[0002] Invention relates to a method for applying an active back bias voltage to NMOS or PMOS transistor well and more particularly to a method of setting the threshold voltage or the leakage current precisely in order to improve speed and control device sub-threshold leakage.

Background of Invention

[0003] Back bias generators were used on NMOS integrated circuits for many years in order to improve performance of large geometry circuits. Many of the early NMOS products made use of a negative voltage to bias the substrate rather than simply grounding in this region. The use of substrate biasing has two benefits; first, the magnitude of this bias voltage

can be automatically regulated to control the threshold voltage of the N-channel transistors because of the body effect or substrate effect on threshold voltage, which prevents an undesired shift to depletion mode. Secondly, biasing the substrate also raises the punch-through voltage of the transistors. Some NMOS products still make use of on-chip-generated substrate biasing to obtain this higher breakdown-voltage advantage.

[0004] U.S. 6,175,263 and U.S. 6,515,534 are examples of biasing schemes focused on CMOS transistors; these inventions lack many of the features and benefits of the present invention.

[0005] At geometries of 0.13 microns and below the sub-threshold source-drain leakage becomes a significant portion of the overall power consumption in CMOS circuits. Power consumption in today's integrated circuits is a major problem.

[0006] A serious problem is that sub-threshold leakage of a small geometry device creates undesired current. This leakage increases as device geometries decrease, note FIG. 1. Drive voltage is squeezed between the maximum Vt and the lowered Vdd.

[0007] As geometries shrink, junction and gate breakdown voltages lower and power supplies voltages must be reduced therefore. As supply voltage

is reduced, the drive voltage margin (Vdd-Vt) is reduced unless the maximum Vt is reduced. Reducing Vt can be accomplished only by tighter and tighter process control; however zero Vt variance is not possible. Also, sub-threshold currents become more and more significant as Vt approaches zero. Finally, temperature variation of sub-threshold currents and Vt itself result in the need for additional "margin" that is simply not available in conventional circuits.

[0008} Mukhopadhyay, et al. (3) describe in detail the impact of various process variations on total leakage in scaled CMOS devices. The authors conclude that ".... (process) parameter variation has significant impact on each leakage component....". The relationship between the threshold voltage, Vt, and sub-threshold leakage, Isub, as a function of various device parameters is detailed in this paper.

Summary of Invention

[0009] Invention resides in actively applying a back bias voltage to wells of N-MOS and P-MOS transistors of small geometry integrated circuits while sensing the sub-threshold leakage current of a reference transistor in the respective well. The active back bias voltage is used to set the threshold voltages or leakage currents precisely in order to improve speed

and at the same time control device sub-threshold leakage. The active back bias generator dynamically supplies a voltage to the well of devices on the integrated circuit. The back bias voltage supplied changes until the sub-threshold leakage current reaches a predetermined level and is then modulated based upon the leakage current sensed and the preset level. This means that if leakage increases with age, temperature, V_{DD} voltage, or other conditions, the bias supply from the active back bias generator will compensate.

Brief Description of Drawings

[0010] FIG. 1 shows how leakage current increases with shrinking geometry, figuratively.

[0011] FIG. 2 figuratively shows how the power supply has ample range for a large geometry device.

[0012] FIG. 3 figuratively shows how the power supply has reduced margin for a small geometry device.

[0013] FIG. 4 figuratively shows how the power supply can have "negative margin" for a small geometry device.

[0014] FIG. 5 figuratively shows how a "passive back bias" solution would improve the leakage but not the Vt distribution for a small geometry device.

[0015] FIG. 6 figuratively shows how a "one bit active back bias" solution improves the leakage and some but insufficient improvement on the Vt distribution for a small geometry device.

[0016] FIG. 7 figuratively shows how a "N-bit active back bias" solution improves the leakage and improves the Vt distribution greatly for a small geometry device.

[0017] FIG. 8 figuratively shows a typical Vt distribution for small geometry devices with the drive margin indicated.

[0018] FIG. 9 figuratively shows a typical Vt distribution for small geometry devices with the drive margin indicated when a N-bit active back bias capability has been added to the circuit.

[0019] FIG. 10 is general system block diagram for implementing present invention on a reference PMOS and NMOS transistor.

[0020] FIG. 11 is a more detailed block diagram of the Active Back Bias Generator.

Detailed Description of Preferred Embodiment

[0021] An active back bias voltage, applied to one or more wells of N-MOS and/or P-MOS transistors of an integrated circuit, is used to set the threshold voltage or the leakage current of the transistors in the well precisely in order to improve speed by optimizing the Vt or conserving power by controlling the sub-threshold leakage current.

[0022] In one embodiment, depending upon the activity of the transistors in a given well for a given period, the back bias generator dynamically modulates the back bias voltage applied to the well to optimize transistor performance based upon a predetermined set of instructions. Typically the instructions optimize the Vt level for speed considerations or minimize the sub-threshold leakage for power saving considerations. Other optimization criteria can be selected. An empirical relationship between Vt and Isub can be employed based upon the particular device and process parameters; a combination of theoretical and empirical relationships is preferred to adjust the back bias level for Vt while measuring or sensing Isub.

[0023] The disclosed invention provides a solution to the conventional problems mentioned above. Using active back biasing, the sub-threshold currents can be accurately and even adaptively, versus temperature, voltage, or other parameters, controlled to a prescribed level set by the design engineer.

[0024] Additional benefits of actively controlling the back bias are also realized:

a) Improved punch-through voltage

b) Lower effective junction capacitance

c) Better "worst-case" performance

d) Multiple, changeable Vt levels on the same chip without a custom process

e) Many of the effects of IC processing variation are eliminated or minimized.

[0025] The invention, termed an "ADOC™" for Active DC Output Control™ technology can be either a separate integrated circuit or an embedded circuit module within a larger integrated circuit. The ADOC™ chip or IC portion precisely controls the well bias of PMOS and NMOS transistors which exhibit undesirable sub-threshold current levels with the

bias of the uncompensated integrated circuit. Multiple ADOC™ chips may be used for large IC's or multiple ADOC™ may be embedded in a large IC.

[0026] FIG. 11 is a block diagram of the ADOC™ integrated circuit. It contains a serial interface for accepting programming of multiple Vt levels in reprogrammable memory. At least two current sensing capabilities, one for a PMOS well and one for a NMOS well are provided. At least two bias voltage setting capabilities, one for a PMOS well and one for a NMOS well are preset. A "logic" portion for accepting instructions through the serial interface is also provided, allowing the user to choose among Vt levels depending upon the application running on the biased chip, for instance a "sleep mode" versus a fast response mode.

[0027] In alternative embodiments one or more Isub levels in combination with one or more Vt levels can be stored and then chosen based upon one or more instructions. Alternatively levels for Isub and Vt can be determined based upon design and process parameters and configured into the circuit at the mask level so that no additional instruction need be given; changing of these levels is then not possible after the fabrication step unless additional circuitry is used.

[0028] Leakage reduction is accomplished by monitoring an input, in one case a current from the IC being controlled. The current from the IC must

be dependent on the leakage current of devices in the same well, PMOS or NMOS, on the IC. This current will then naturally decrease with increased back bias. The ADOC™ adjusts an output voltage, which is the back bias voltage for the well being monitored, until the current returning from the IC achieves a pre-set value which has been programmed into a circuit element. This voltage is then dynamically maintained about the target voltage that generated the programmed current value. Even when conditions which affect the leakage current change such as temperature, supply voltage, age, etc., the closed-loop ADOC™ function adjusts the back bias voltage until the leakage current is again at the pre-set target. The pre-set target value can be set in the prototype phase using a Summit supplied GUI, graphical user interface. The GUI then issues a code which is used in production to set the current before the part is shipped. If desired, the current can be programmed post the printed circuit board stuffing level using an alternative interface

[0029] The ADOC™'s active back bias generator applies a voltage to a well of devices on the small geometry integrated circuit. Wells connected to each other need only one, optimally placed, reference transistor for the active back bias generator to monitor. Unconnected wells require their own reference transistor for a dedicated active back bias generator to monitor. Alternatively when unconnected wells are well characterized such that the back bias to achieve a given Isub, and consequently a certain

Vt, in one well is a known function of the back bias to achieve the same parameters in a different well then only one reference transistor is needed. The dynamically applied back bias voltages to the different wells is adjusted based upon the known relationship of the measured reference transistor and the unmonitored wells. The maximum back bias voltage applied is limited based upon theoretical and empirical considerations. "Small geometry" as used here is a relative term and is not meant to be limiting to the invention. In general the benefits of this invention will be realized in integrated circuits with geometries of 0.25 microns and smaller.

[0030] In an alternative embodiment one ADOC™ chip or embedded portion is switched between various wells based upon the activity level of the transistors in the well. If the transistors in one well are in a non-active or unpowered state then no ADOC™ control is required and an ADOC™ associated with that well may be switched to dynamically control a powered well.

[0031] Foregoing described embodiments of the invention are provided as illustrations and descriptions. They are not intended to limit the invention to precise form described. In particular, it is contemplated that functional implementation of invention described herein may be implemented

equivalently in hardware, software, firmware, and/or other available functional components or building blocks. Other variations and embodiments are possible in light of above teachings, and it is thus intended that the scope of invention not be limited by this Detailed Description, but rather by Claims following.